LINEAR (AUDIO)



COMPLEX SOUND GENERATOR



GENERAL DESCRIPTION

The SN76495 complex sound generator is a monolithic chip combining both analog (bipolar) and digital (I2L) circuitry. It includes a noise generator, a voltage-controlled oscillator (VCO), and a super-low-frequency oscillator (SLF) together with a noise filter, mixer, audio amplifier, and control circuitry to provide noise, tone, or low-frequency sounds and any combinations of these. Programming is accomplished via control inputs and user-defined external components, which allows a wide variety of sound to be created and tailored for particular applications. This device may be used in a variety of applications requiring audio feedback to the operator.

Operation is from a 7.5 volts to 10.5 volt supply applied to a built-in regulator through the V_{CC} terminal, in which case a regulated five volts is available from the Vreg terminal to power a small amount of external circuitry, or to provide a high-logic-level voltage to logic inputs.

FEATURES

- Generates noise, tone, or low frequency based sounds, or combinations of these
- Sounds are defined by user via external components
- Allows custom sounds to be created easily
- Low power requirements
- Allows multiple sound system
- Compatible with microprocessor systems
- On board 125 mW audio amplifier

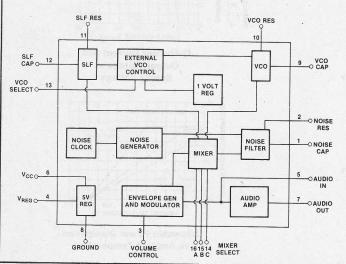
APPLICATIONS

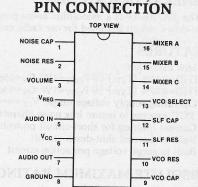
- Arcade Games
- Video Games
- Pinball Games
- Toys
- Timers
- Alarms

ABSOLUTE MAXIMUM RATINGS

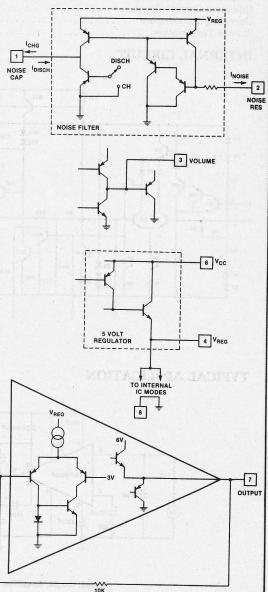
Supply Voltage (V _{CC} 12 V
12 V
Input Voltage: Logic Input 12 V
Capacitor Input 5.0 V
Resistor Input
Operating Temperature Range
Storage Temperature Range
NOTE 1: All voltage values are with respect to package ground terminal.

BLOCK DIAGRAM









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AUDIO

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OPERATION

Super Low Frequency Oscillator (SLF)

The SLF is normally operated in the range of 0.1 Hz to 30 hertz, but will operate up to 20 kHz. The frequency is determined by two external components, the SLF control resistor (Rslf) at pin 11 at ground and the SLF control capacitor (Cslf) at pin 12 at ground according to the following equation:

Equation 1: SLF Frequency (Hz) ~ .66/(9Kohm+Rslf)xCslf at Vreg=5V

The SLF supplies two signals to other parts of the device. It feeds a 50% duty cycle square wave to the mixer, and it feeds a triangular wave to the external VCO of SLF select logic, where, if VCO select (pin 13) is at a low logic level, it is fed through to the VCO to modulate the frequency of that oscillator.

Voltage Controlled Oscillator (VCO)

The VCO produces a tone output whose frequency is dependent upon the voltage at the input of the VCO. This controlling voltage may be either the SLF output described above, an internal voltage producing a constant tone, or externally by placing a voltage on the SLF capacitor pin. The higher the voltage applied to the VCO, the lower the frequency of the VCO output.

The first mode, VCO controlled by SLF, is selected by placing the VCO select pin low and supplying both the VCO capacitor (CVCO) at pin 9 at ground the the VCO resistor (RVCO) at pin 10 at ground. Minimum frequency of the VCO is determined by the following equation:

Equation 2: Minimum VCO Frequency (Hz) ~0.60/(9Kohm+RVCO) × CVCO

The frequency range of the VCO is internally determined at an approximate ratio of 10:1, so that maximum frequency of the VCO will be approximately ten times the minimum frequency determined by the external components RVCO and CVCO.

The second method of supplying a control voltage for the VCO is to use an internal voltage preset at 1 volt. This mode is selected by taking VCO select to a high level. In this mode, the VCO puts out a constant tone determined by CVCO and RVCO in this relationship:

Equation 3: fVCO ~ 1.45/(RVCO + 9Kohn) × CVCO × 0.9V) Hz

A third method of controlling the voltage to the VCO is to apply the controlling voltage (Vext) to the SLF capacitor pin. This voltage level (0 to 2.30 volts) will determine the output frequency of the VCO. Output frequency in this mode is determined by this relationship:

Equation 4: fVCO ~ 1.45/(RVCO + 9Kohn) × CVCO × (Vext - .1V) Hz

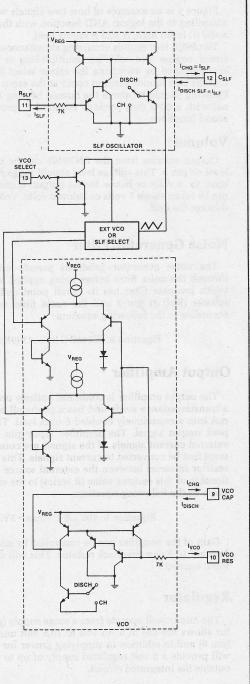
Mixer

The mixer logic selects one or a combination of the inputs from the generators and feeds the output to the amplifier. The mixer performs a logical AND function on these sounds; therefore, the output of the mixer is not a combination of simultaneous sounds. The output of the mixer is determined by the logic levels at the mixer select inputs as shown in Table 1.

TABLE 1

	MIXER SELECTS INPUTS		
MIXER OUTPUT	C (PIN 14)	B (PIN 15)	A PIN 16)
VCO	L	L	L
SLF	L	L	Н
NOISE	L	Н	L
VCO/NOISE	L	Н	Н
SLF/NOISE	H	L	L
SLF/VCO/NOISE	H ·	L	Н
SLF/VCO	Н	Н	L
INHIBIT	H	Н	Н





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Mixer (Cont'd)

Figure 1 is an example of how two signals would be combined by the mixer according to the logical AND function with the mixer select times set for SLF/ noise (C input high, A and B inputs low).

To obtain two sounds occurring simultaneously (e.g., car engine and siren or steam engine and whistle), multiplexing is required. The multiplexing is accomplished by switching the mixer select lines at a sufficiently rapid rate that the two sounds seem to occur at the same time. The frequency of the multiplexing should be above the human hearing range. A multiplexing drive signal with a 50% duty cycle is required to provide equal amplitudes for both sound functions.

Volume

Output volume from the SN76495 can be controlled by varying a voltage level on pin 3. This voltage level should range from 3.5 volts, for maximum volume, to .4 volts or below for no output. Under no circumstances should this pin be taken above 5 volts or below 0 volts. Voltages outside of this range could damage the unit.

Noise Generator/Filter

The noise generator produces pseudo-random white noise that passes through the noise filter before being applied to the mixer. The variable-bandwidth low-pass filter has its cutoff point defined by the noise filter control resister (Rnf) at pin 2 and the noise filter control capacitor (Cnf) at pin 1 according to the following equation:

Equation 5: fCutoff (Hz) = .43/(9Kohm + Rnf) × Cnf

Output Amplifier

The output amplifier is contained entirely on chip. The amplifier operates in a transimpedance mode and has a push-pull output capable of delivering 125 mA into a capacitively coupled 8 ohm load. This produces a two volt peak to peak output signal. The amplifier input (pin 5) can be used to sum several external current signals. If the signals are composed of a varying voltage they must first be converted to current signals. This can be accomplished by using a resistor in series between the external source and the input (pin 5). The relationship of this resistor value (R series) to the external signal voltage (V max) is given by the following equation:

Equation 6: 100 μ A < Vmax - 3V/Rseries < 100 μ A

Gain of the amplifier can be controlled by adding a resistor in parallel to the internal 10 Kohm feedback resistor. This will decrease gain and allow a larger input current.

Regulator

The circuit will operate from a singe supply (pin 6). An internal 5 volt regulator allows the use of a 7.5 volt to 10.5 volt unregulated supply applied to V_{CC} (pin 6) and in addition to supplying power for the chip, the internal regulator will provide a 5 volt regulated supply of up to 5 mA from Vreg (pin 4) for use outside the integrated circuit.

INTERNAL CIRCUITS (Cont'd)

